

Applicant : David Qiang Meng
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Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A computer-implemented method comprising:
partitioning a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.
2. (Currently Amended) The computer-implemented method of claim 1, further comprising:
partitioning a memory entry in the first group of memory entries into sub-entries.
3. (Currently Amended) The computer-implemented method of claim 1, further comprising:
selecting the first group of memory entries for accessing in parallel.
4. (Currently Amended) The computer-implemented method of claim 1 wherein the memory device is included in a multithreaded engine of a packet processor.
5. (Currently Amended) The computer-implemented method of claim 1 wherein the first group of memory entries store a first type of data and the second group of memory entries store a second type of data.
6. (Currently Amended) The computer-implemented method of claim 2 wherein the memory entry includes at least two subentries.
7. (Currently Amended) The computer-implemented method of claim 2 wherein the memory entry includes a combination of subentries.

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8. (Currently Amended) A computer program product, tangibly embodied in an information carrier a computer readable medium, the computer program product being operable to cause a machine to:

partition a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.

9. (Original) The computer program product of claim 8 being further operable to cause a machine to:

partition a memory entry in the first group of memory entries into sub-entries.

10. (Original) The computer program product of claim 8 being further operable to cause a machine to:

select the first group of memory entries for accessing in parallel.

11. (Currently Amended) A The computer program product of claim 8 wherein the memory device is included in a multithreaded engine of a packet processor.

12. (Original) The computer program product of claim 8 wherein the first group of memory entries store a first type of data and the second group of memory entries store a second type of data.

13. (Original) The computer program product of claim 9 wherein the memory entry includes at least two subentries.

14. (Original) The computer program product of claim 9 wherein the memory entry includes a combination of subentries.

15. (Original) A content-addressable memory (CAM) manager comprises:
a process to partition a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.

16. (Original) The CAM manager of claim 15 further comprising:

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a process to partition a memory entry in the first group of memory entries into sub-entries.

17. (Original) The CAM manager of claim 15 further comprising:

a process to select the first group of memory entries for accessing in parallel.

18. (Original) A system comprising:

a memory device capable of being partitioned to produce a first group of memory entries that is accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.

19. (Original) The system of claim 18 wherein a memory entry in the first group of memory entries is capable of being partitioned into sub-entries.

20. (Original) The system of claim 18 wherein the first group of memory entries is further capable of being selected for accessing in parallel.

21. (Original) A packet forwarding device comprising:

an input port for receiving a packet;

and output port for delivering the received packet; and

a memory device capable of being partitioned to produce a first group of memory entries that is accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.

22. (Original) The packet forwarding device of claim 21 wherein a memory entry in the first group of memory entries is capable of being partitioned into sub-entries.

23. (Original) The packet forwarding device of claim 21 wherein the first group of memory entries is further capable of being selected for accessing in parallel.

24. (Original) A content-addressable memory (CAM) comprising:

a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the CAM that is accessible in parallel.

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25. (Original) The CAM of claim 24 wherein a memory entry in the first group of memory entries is capable of being partitioned into sub-entries.

26. (Original) The CAM of claim 24 wherein the first group of memory entries is further capable of being selected for accessing in parallel.